AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 5, line 13, with the following rewritten paragraph:

According to Claim 1 of the present invention, there is provided a filter coefficient adjusting circuit which includes an FIR filter which makes an input signal subjected to a filtering process according to an equalization coefficient, a PLL which extracts a clock synchronized with the input signal using an output from the FIR filter, an equalization performance detecting unit which detects an equalization performance of the FIR filter, and an equalization coefficient determining unit which ~~determines the equalization coefficient of the FIR filter according to an output value of the equalization performance detecting unit~~ weights the previously-set equalization coefficient of the FIR filter, for left and right taps, with respect to a center tap when the number of taps in the FIR filter is an odd number, and with respect to a central delay line when the number of taps in the FIR filter is an even number, according to an output value of the equalization performance detecting unit, and outputs the weighted value.

Please replace the paragraph at page 5, line 24, with the following rewritten paragraph:

Therefore, it is possible to simplify the control within the circuit, and ~~optimize the group delay of the input signal~~ adjust the group delay of the FIR filter by weighting left and right equalization coefficients of the FIR filter so that the output value of the equalization performance detecting unit is optimized according to the characteristics of the input signal without providing additional circuits, thereby enhancing the reproduction performance.

Please replace the paragraph at page 6, line 4, with the following rewritten paragraph:

According to Claim 2 of the present invention, there is provided a filter coefficient adjusting circuit as defined in Claim 1, wherein the equalization coefficient

determining unit ~~outputs a previously set initial value as the equalization coefficient of the FIR filter~~ weights the equalization coefficient of the FIR filter symmetrically, with respect to a center tap when the number of taps in the FIR filter is an odd number, and with respect to a central delay line when the number of taps in the FIR filter is an even number before the PLL reaches the locked state.

Please replace the paragraph at page 6, line 10, with the following rewritten paragraph:

Therefore, ~~since the jitter value becomes stationary after the PLL has locked, it is possible to smoothly carry out a search~~ by symmetrically performing the weighting of the equalization coefficients before the PLL reaches the locked state, it is possible to smoothly perform a subsequent search for an optimum value for the equalization coefficient.

Please replace the paragraph at page 14, line 12, with the following rewritten paragraph:

Fig.3 is a diagram illustrating a detailed structure of the ~~filter coefficient adjusting circuit 2~~ coefficient adjusting circuit 2 in the filter coefficient adjusting circuit of Fig.1(a).